Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1-24 have been amended.

Listing of Claims:

1. (Currently amended) A method, comprising:

monitoring at least one waiting instruction in an instruction window, wherein the waiting instruction includes a reference to a physical register;

~~tracking one or more physical register references associated with one or more physical registers called on by said at least one instruction;~~

~~determining~~ incrementing a reference count for said ~~one or more~~ physical register[[s]] based on said ~~one or more physical register~~ reference[[s]];

~~determining a potential significance for data of said one or more physical registers based on said reference count~~ utilizing said reference count to determine the potential significance of data in said physical register to future instructions; and

entering said data into ~~updating~~ at least one register cache according to said potential significance.

2. (Currently amended) The method of claim 1, further comprising:

incrementing said reference count once for each additional reference to said physical register in the instruction window.

~~inserting said data of said one or more physical registers into said at least one register cache according to said potential significance~~.

3. (Currently amended) The method of claim [[2]]1, wherein said ~~inserting~~ entering said data is conditional on said potential significance being high.

4. (Currently amended) The method of claim [[2]]1, wherein said ~~inserting~~ entering said data is conditional on said potential significance being low.

5. (Currently amended) The method of claim [[2]]1, wherein said entering further comprises inserting data ~~is inserted~~ into an empty slot in said at least one register cache.

6. (Currently amended) The method of claim [[2]]1, further comprising:

selecting previous data from a slot in said at least one register cache according to the potential significance of said previous data; and

evicting said previous data from said slot in said at least one register cache prior to said inserting said data.

7. (Currently amended) The method of claim 1, ~~said tracking one or more physical register references further comprising~~ wherein:

said waiting instruction includes a reference to a second physical register; and

said incrementing further comprises incrementing a second reference count for said second physical register based on said reference to the second physical register.

~~associating at least one physical register identifier with said at least one instruction;~~

~~associating at least one counter with said physical register identifier; and~~

~~varying said at least one counter for each of said physical register references according to said at least one instruction.~~

8. (Currently amended) The method of claim [[7]]1, wherein ~~said at least one counter is incremented for each of said at least one physical register references~~:

said utilizing is performed responsive to a demand miss.

9. (Currently amended) An apparatus, comprising:

one or more physical registers to store data associated with a plurality of instructions;

an instruction window ~~of~~ to hold the plurality of instructions, the plurality of instructions including at least one waiting instruction whose data is not yet available in the physical registers;

~~one or more physical registers to store data associated with said plurality of at least one instructions;~~

a counter look-up table to track ~~one or more~~ the number of ~~physical register~~ references ~~associated with~~ to each of said one or more physical registers in the instruction window;

a reference count circuit to determine ~~a reference count for said one or more physical registers and~~ a potential significance for data of said one or more physical registers based on said number of references ~~count~~; and

at least one register cache, wherein said reference count circuit is to enter data into ~~updates~~ said at least one register cache according to said potential significance.

10. (Currently amended) The apparatus of claim 9, wherein at least one register cache, wherein said reference count circuit is further to enter ~~inserts~~ said data of said one or more physical registers into said at least one register cache according to said potential significance.

11. (Currently amended) The apparatus of claim [[10]]9, wherein said reference count circuit is to enter~~inserts~~ said data when said potential significance is high.

12. (Currently amended) The apparatus of claim [[10]]9, wherein said reference count circuit ~~inserts~~ is to insert said data when said potential significance is low.

13. (Currently amended) The apparatus of claim [[10]]9, wherein said reference count circuit ~~inserts~~ is to insert said data into an empty slot in said at least one register cache.

14. (Currently amended) The apparatus of claim [[10]]9, wherein said reference count circuit ~~selects~~ is to select and evict ~~and evicts~~ previous data from a slot in said at least one register cache according to a potential significance of said previous data prior to inserting said data.

15. (Currently amended) The apparatus of claim 9, said counter look-up table further comprising:

at least one physical register identifier ~~associated with said at least one instruction~~; and

at least one counter associated with said physical register identifier, wherein said at least one counter is to indicate the number of references to said physical register in the instructions of

the instruction windowvaries for each of said physical register references according to said at least one instruction.

16. (Currently amended) The apparatus of claim 15, wherein said reference count circuit is further to increment the counter counter is incremented for each of said at least one physical register references.

17. (Currently amended) A system, comprising:

a processor including an instruction window to hold a plurality of instructions, the plurality to include of at least one future instruction, one or more physical registers to store data associated with said at least one future instruction, a counter look-up table to track one or more physical register references in the instruction window associated with to said one or more physical registers, a reference count circuit to determine a reference count for said one or more physical registers and a potential significance for data of said one or more physical registers based on said physical register references count, and at least one register cache, wherein said reference count circuit updates is to enter data into said at least one register cache according to said potential significance;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

18. (Currently amended) The system of claim 17, wherein said reference count circuit is to enter inserts said data of said one or more physical registers into said at least one register cache

according to said potential significance to the plurality of instructions in the instruction window, including to said future instruction.

19. (Currently amended) The system of claim [[18]]17, wherein said reference count circuit ~~inserts~~ is to enter said data ~~when~~ responsive to said potential significance being ~~is~~ high.

20. (Currently amended) The system of claim [[18]]17, wherein said reference count circuit ~~inserts~~ is to enter said data ~~when~~ responsive to said potential significance being ~~is~~ low.

21. (Currently amended) The system of claim [[18]]17, wherein said reference count circuit ~~inserts~~ is further to enter said data into an empty slot in said at least one register cache.

22. (Currently amended) The system of claim [[18]]17, wherein said reference count circuit is further to select and evict ~~selects and evicts~~ previous data from a slot in said at least one register cache according to a potential significance of said previous data prior to inserting said data.

23. (Currently amended) The system of claim 17, ~~said counter look-up table~~ further comprising:

one or more additional physical registers to store data associated with the plurality of instructions;

wherein said counter look-up table is further to track one or more physical register references in the instruction window to said additional physical registers.

~~at least one physical register identifier associated with said at least one instruction; and~~

~~at least one counter associated with said physical register identifier, wherein said at least one counter varies for each of said physical register references according to said at least one instruction.~~

24. (Currently amended) The system of claim [[23]]17, wherein said reference count circuit is further to increment said counter ~~is incremented~~ for each of said at least one physical register references.